UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,638	03/30/2001	Ryou Nakagaki	16869P023300	6928

20350 7590 09/23/2005

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
SHAPIRO, JEFFERY A	

ART UNIT	PAPER NUMBER
3653	

DATE MAILED: 09/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,638	NAKAGAKI ET AL.	
	Examiner	Art Unit	
	Jeffrey A. Shapiro	3653	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11,23-28 and 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11,23-28 and 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-11, 23-25, 28 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stephan et al (US 6,338,001 B1) in view of Hance (US 6,574,359 B1) and further in view of Chen (US 5,862,055), and further in view of Gleason et al (US 6,456,899 B1), further in view of Nishimura et al (US 6,456,899 B1), further in view of Kumagai (US 5,394,481) and still further in view of Jarvis et al US 6,297,644 B1). Stephan et al discloses the following.

As described in Claims 1, 6, 9, 11 and 30-32;

a. imaging an inspected object (204) (see col. 5, lines 10-16);

b. extracting an image of a defect candidate from an image obtained by said imaging step (see col. 5, lines 10-16);

c. classifying said extracted defect candidate image into a first category (at least one defect type) (see col. 5, lines 16-20, noting "defects are classed as to type and size");

d. classifying said extracted defect candidate into a second category (evaluation of defect criticality) (see col. 5, lines 20-27, noting that criticality is construed as a kill ratio);

e. displaying on a screen said extracted defect candidate image *together with first and second classification information, said first classification information relating to* said first category, *said second classification information relating to* said second category;

(See figure 4, noting that it would have been obvious for the image data to be presented along with the defect data and kill ratio data, for example, which describes it, *as one ordinarily skilled in the art would recognize that* effective review and comparison of the chip defects with what an ideal example of such chip features should be (see col. 4, lines 65-67 and col. 5, lines 1-10) would require a visual representation of the particular defect so that appropriate changes can be made to the process or design of the chip);

f. *said step of classifying said extracted defect candidate image into said second category is performed by comparing a circuit pattern area and a defect area, said circuit pattern area being obtained from a reference image and said defect area being obtained from said imaging step*;

(Regarding using a comparison image, note that it would have been obvious to one of ordinarily skill in the art to use a comparison image from an ideal circuit pattern to compare to a defect area image. Otherwise, there is no way to determine the bounds of roundness, straightness, etc., of metal lines and structures created on the wafers, as described in Stephan et al at col. 1, lines 42-47. One of ordinary skilled in the art, in

context to the teachings discussed in Stephan et al and cited above, would recognize that such comparison of an image of various chip defects and an actual ideal chip feature would be required in order to determine whether or not the chip features which are defective are within acceptable tolerances. See also Chen et al (US 5,862,055), figure 3, step (304), incorporated by reference in Stephan et al at col. 2, lines 43-49. Note that each defect can be construed as a separate classification based on a classification code. See Chen at col. 1, lines 44-67, col. 2, lines 1-46, 63-67 and col. 3, lines 1-3. Also note as a further example, Gleason et al, at col. 2, lines 58-63 which describes use of a reference image (21) for comparison with defect image (22).

Stephan does not expressly disclose, but Hance discloses using two detectors (24a and b) disposed at angles to said object and detectors (18) disposed above said object. See Hance, figure 1.

Both Stephan and Hance are considered to be analogous art because they both concern semiconductor defect analysis equipment.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have used multiple detectors at angles to the semiconductor being inspected as well as detectors disposed above the semiconductor.

The suggestion/motivation would have been to capture rays scattered from a semiconductor defect in all directions, and therefore prevent defect blind spots from

developing. See col. 5, lines 35-67 and col. 6, lines 1-12, and particularly, col. 6, lines 3-6.

Further, note that evaluating overlap areas between the defect area and the reference circuit area are considered to be obvious, and that comparison of the two area images without overlay are considered to be functional equivalents.

As described in Claims 3, 4, 26 and 28;

g. said first category relates to defect criticality;

h. said second category relates to defect criticality;

i. said second category relates to defect type;

j. said first category relates to defect type;

(Note that regardless of whether or not the criticality or the defect type is determined first, the process result is substantially the same as Applicants' process. Note also that the location of a particular defect is captured by the scanner, which one ordinarily skilled would find obvious to use for determining criticality, since criticality can be defined in terms of the location of the defect. See col. 1, lines 61-64.)

As described in Claim 9;

k. said second category relating to predicted yield from said inspected object (316);

Stephan et al discloses the system described above. Stephan does not expressly disclose, but Gleason discloses the following;

As described in Claims 2, 7, 10 and 23-25;

l. said imaging of said inspected object is performed by illuminating and scanning an electron beam focused on said inspected object and detecting, in synchronization with said scanning, secondary electrons generated from said inspected object by said illumination (note that it is obvious to provide an electron beam for scanning, said electron beam necessarily producing secondary electrons from the surface it is directed at—see Gleason et al, for example, at col. 2, lines 58-63);

Both Stephan and Gleason are analogous art because they both concern automated semiconductor wafer inspection and defect classification systems.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have used an electron beam in the form of a scanning electron microscope (SEM) for inspecting the wafer.

The suggestion/motivation would have been to generate a reference image and a defect image. See col. 2, lines 58-63 of Gleason. Note also that Stephan discloses a semiconductor wafer inspection system, and that it would be obvious to one ordinarily skilled in the art to have used an SEM to obtain such images. See col. 2, lines 4-10 of Stephan.

Stephan et al discloses the system described above. Stephan does not expressly disclose, but Nishimura et al and Kumagai disclose the following;

As described in Claims 1, 5, 6, 8, 9, 27 and 33;

m. said defect type includes one or more of the following: particle defects, flaw defects, circuit pattern short defects, circuit pattern open defects and voltage contrast defects; (Note that an inspection system such as that of Steffan et al determines such defects, as one ordinarily skilled in the art would recognize them as well-known semiconductor circuit defects found in wafers during manufacturing. Note that these defects are considered to be functional equivalents of each other, at the very least. See also Nishimura et al, figure 3 and Kumagai et al, figure 9.)

Stephan does not expressly disclose, but Nishimura et al and Jarvis disclose the following;

As described in Claims 1, 5, 9 and 33;

n. calculating third information relating to voltage contrast of the defect candidate; (Note that this is considered to be a functional equivalent of other dimensional defects, and are related to shorts circuits or connection faults, as described in figure 3 of Nishimura et al. See also Jarvis et al (US 6,297,644), last four lines of abstract and figures 9a, 9b, 10a, 10b and

11, illustrating short circuit situations and col. 2, lines 66 and 67, col. 3, lines 1-9, and col. 7, lines 58-60, mentioning use of a scanning electron microscope (SEM) to perform such voltage contrast studies of defects. Note also that Stephan, at col. 2, lines 4-10, indicate that SEM is one of the pieces of equipment used for inspection of wafers.

Stephan, Nishimura, Kumagai and Jarvis are analogous art because they all concern automated semiconductor wafer inspection and defect classification systems.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have inspected a wafer for particle defects, flaw defects, circuit pattern short defects, circuit pattern open defects and voltage contrast defects.

The suggestion/motivation would have been to obtain "critical dimensions, that is, dimensions that can affect the performance of the semiconductor chip." See col. 1, lines 42-47 of Stephan. Note again, that figure 9 of Kumagai discloses various types of defects charted, such as holes, spots and breaks. Figure 3 of Nishimura discloses images of various connection faults and short circuits, said short circuits and connection faults construed as voltage contrast defects.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have calculated third information relating to voltage contrast of the defect candidate;.

The suggestion/motivation would have been to obtain "critical dimensions, that is, dimensions that can affect the performance of the semiconductor chip." See col. 1,

lines 42-47 of Stephan. Note again, figure 3 of Nishimura discloses images of various connection faults and short circuits, said short circuits and connection faults construed as voltage contrast defects. Jarvis again discloses at col. 2, lines 50-67 and col. 3, lines 1-9, the use of "voltage contrast inspection" in order to identify catastrophic defects in semiconductor wafers.

Response to Arguments

3. Applicant's arguments filed 7/11/05 have been fully considered but they are not persuasive. Claims 1, 3-11, 23-28 and 33 have been considered above.

Applicant asserts that the addition of the limitations regarding use of a kill ratio in addition to a defect surface shape information, pattern defect information, and voltage contrast defect information, overcomes the prior art. Jarvis describes use of voltage contrast, Hance discloses use of the topography/shape of the defect (28), in Hance, col. 5, lines 36-40, and Kumagai discloses use of pattern data, that is, the location of particular defects on the wafer, in Kumagai, figure 9, for example. It would have been obvious to one of ordinary skill in the art to have used these as well as other measurement parameters together so as to accurately and efficiently determine the cause of wafer semiconductor device failure. See also Kumagai, col. 1, lines 10-38, Hance, col. 1, lines 5-50 and Jarvis, col. 1, lines 5-67, col. 2, lines 1-10 and 50-67, and col. 3, lines 1-21.

In fact, Stephan illustrates in figure 3, element (310), in which a type of defect is identified. Voltage shorting or lack of conductivity is one type of defect, while surface topography, that is, pitting or excess material deposit, is a second type. Kumagai

discloses use of pattern data, discussed above. Since Stephan discloses use of statistical yield predictions at element (316), figure 3, it would have further been obvious to use such pattern data in addition to topography and voltage data. Additionally, Stephan discloses at col. 1, lines 5-17, that yield prediction is the goal of his system. One ordinarily skilled in the art would find it logical that in order to predict the yield from a wafer more accurately, varying forms of data are required. The more types of data gathered, the more accurate the yield prediction becomes. Therefore, in view of Hance, Jarvis and Kumagai, it would have been obvious to one of ordinary skill in the art to have used all three of these types of data in Stephan's system so as to accurately predict wafer yields.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey A. Shapiro whose telephone number is (571)272-6943. The examiner can normally be reached on Monday-Friday, 9:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald P. Walsh can be reached on (571)272-6944. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeffrey A. Shapiro
Examiner
Art Unit 3653

September 19, 2005

DONALD P. WALSH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 3600